Summary nanoscience and nanotechnology – Ivo Meijers

Lecture 1 - Introduction

Nanotechnology - Nanotechnology involves manipulating matter at unprecedentedly small scales to create new or improved products that can be used in a wide variety of ways.

Scaling law:

- Smaller things are less effected by volume dependent phenomena: mass, inertia
- Smaller things are more effected by surface area dependent phenomena: contact forces and heat transfer.
- A volume decreases much faster than an area

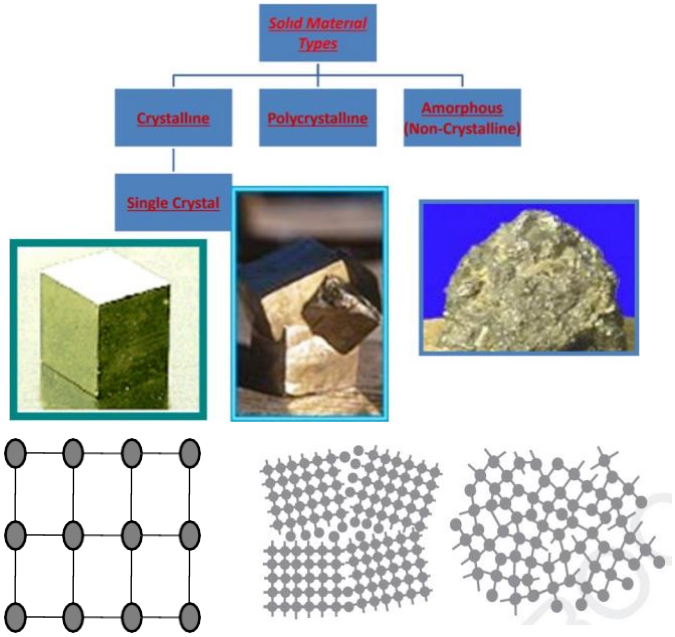
Lecture 2 & 3 – Crystal structures and fundamentals

Nano fabrics are made under specific circumstances in *clean rooms*, in which the following factors are controlled: temperature, humidity, air cleanliness, room pressure, air movement and lighting.

Silicon is the most used nano fabric. Silicon has the following characteristics:

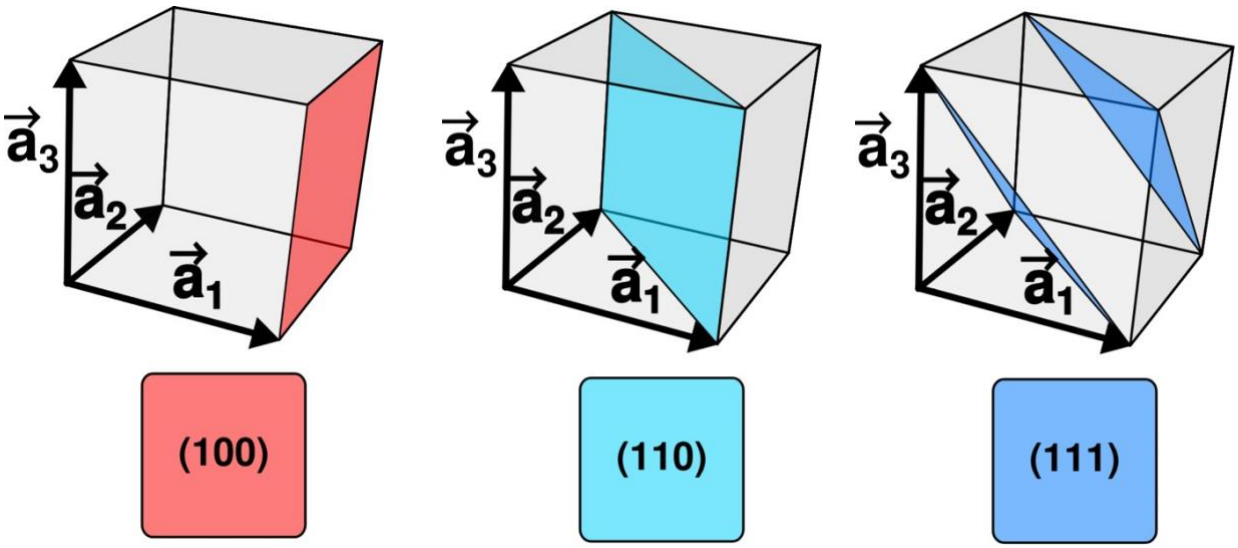
- Good mechanical material
- Good thermal material
- Good semi-conductor
- Optically smooth and flat
- Transparent in infrared
- Known inside out

Types of silicon materials:



Crystal structures:

The planes and directions of a crystal structure is defined by the x,y,z-coordination (Miller-index). Examples:

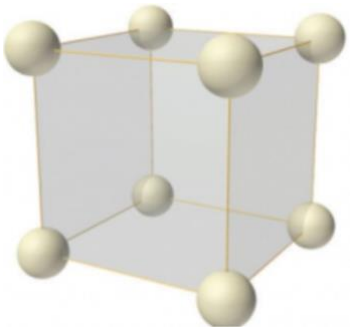


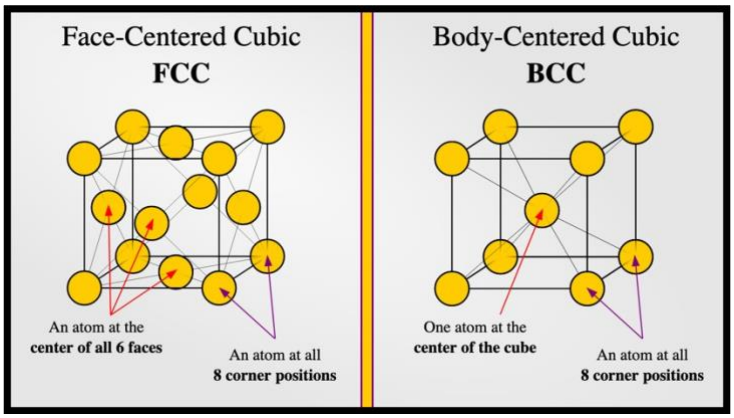
The Miller-index has influence on the following factors: *Optical properties, Reactivity, Surface Tension, Dislocation.*

Five different types of crystal systems:

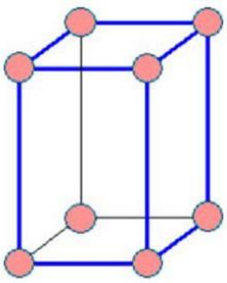
Cubic:

Simple cubic

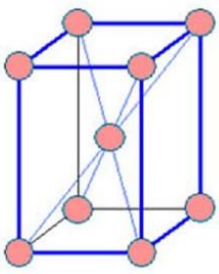




Tetragonal:



Simple Tetragonal



Body-centered Tetragonal (BCT)

Atom Packaging Factor (APF) = $\frac{Volume\ of\ Atoms}{Volume\ of\ unit\ cell}$ planar density = $\frac{Number\ of\ atoms\ on\ plane}{Area\ of\ the\ plane}$

Theoretical density = $\frac{n*A}{Vc*Na}$ where n = #atoms/unit cell, A = atomic weight, Vc = volume/unit cell, Na = Avogadro's number

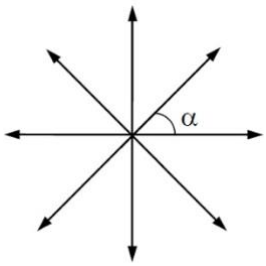
Coordination number - the number of nearest neighbouring atoms to a particular atom in a crystal. Coordination number → FCC = 12, BCC = 8

Crystalline type	Atoms/cell	APF	Coordination number	Radius
SC	1	0,52	6	a/2
BCC	(8*(1/8) + 1) = 2	0,68	8	$\frac{\sqrt{3}a}{4}$
FCC	(8 *(1/8) + 6 * (1/2)) = 4	0,74	12	$a/2\sqrt{2}$
Diamond	(8*(1/8) + 6 * (1/2) + 4) = 8	0,34	-	$\frac{\sqrt{3}a}{8}$

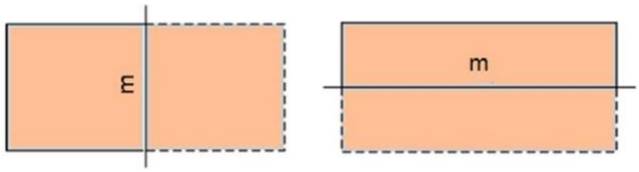
<u>Three different kinds of Symmetry</u>**:**

1. Translation:
   The first point is repeated at equal distances along a line by a translation uT, where T is the translation vector and u is an integer.

2. Rotation:
   Symmetry around a point:



3. Reflection/mirror:



<u>Single crystal perfection:</u>

A crystal is considered as perfect if all atoms have identical surroundings. Real crystals are not perfect. At the surface of a crystal atomic bonds terminate and therefore the surface is imperfect.

Crystal defects:

1. Point imperfections:
   A defect where one atom is missing (vacancy). This could occur through levels of an atom due to high temperatures. If a pair of anion and catio from an ionic crystal, it's called *Schottky-imperfection*.

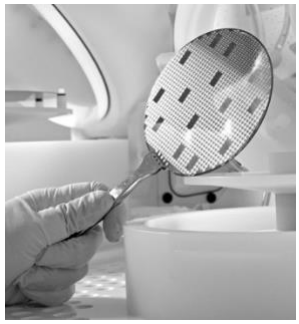
2. Substitutional impurity:
   A foreign atom substitutes at the place of a vacancy.

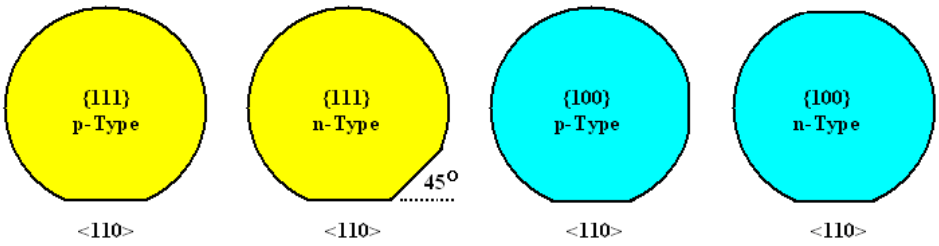
3. Interstitial impurity:
   A small sized atom occupies void space between the parent atoms.

Lecture 4 – Silicon wafers

Silicon wafers:

A wafer is a thin slice of a semi-conductor (most often Silicon). This wafer serves as a substrate for devices (dies), such as resistors and diodes. These wafers vary in diameter from 1 to 12 inch. A wafer could be cut in several ways, using the Miller-index:





A p-type silicon wafer is always doped in Boron (B), where a n-type silicon wafer is doped in Res: .001-.005 Arsenic (As), Res: .005-.025 Antimony (Sb), Res: >.1 Phosphorous (P). The wafers are cut these ways as orientation for automatic equipment and as an indication of the type and orientation of crystal.

Integrated circuit fabrication has specific demands on a silicon wafer:

- Each silicon wafer must be fabricated with a specific orientation, resistivity, and dopant type which need to meet certain standards
- Defects in the wafers (point, line surface and volume imperfections in the crystals) must be below tolerance
- Impurity concentration of the wafers must be below permissible level (ppm or less) 7 nines purity is required (99.99999% pure)
- Thickness of the wafers must be within tolerance (±25µm or less)
- (1,0,0) or desired wafer orientation parallel to the surface within 2 degrees.
- Dopants and resistivity within tolerance (<10 ohm-cm)

Process of creating a silicon wafer:

Step 1: Producing Metallurgical grade silicon (MGS, often Silicon (Si))

Quartzite or sand (SiO_2) is mixed with coal, coke or wood chips and the mixture is heated to temperatures beyond the melting point of silicon (1500-2000 ^{0}C). This process is conducted in an electrode arc furnace. The MGS often contains impurities as Al and Fe. $SiO_2 + C_2 \rightarrow Si + 2CO$

Step 2: Siemen's process to form Electronic Grade silicon (EGS)

Si is reacted with HCl gas to form trichlorosilane. This process is conducted in a fluidized bed reactor at 300 ^{0}C. $Si + 3HCl \rightarrow SiHCl_3 + H_2$

The HCl from SiHCl is removed by using H_2. This causes the number of impurities to decrease. In EGS there are far lesser impurities than in MGS. $2SiHCl_3 + 2H_2 \rightarrow 2Si + 6\ HCl$

Step 3: Single crystal silicon wafer formation

This step causes further purification and the formation of perfect monocrystalline (single crystal) silicon in wafer form. Two techniques are distinguished:

Czochralski technique: Most predominant technique for manufacturing single crystals. It is widely used in IC industry since it is the best method to obtain defect free single crystalline wafers.

Four main components of the process (https://www.youtube.com/watch?v=AMgQ1-HdElM):

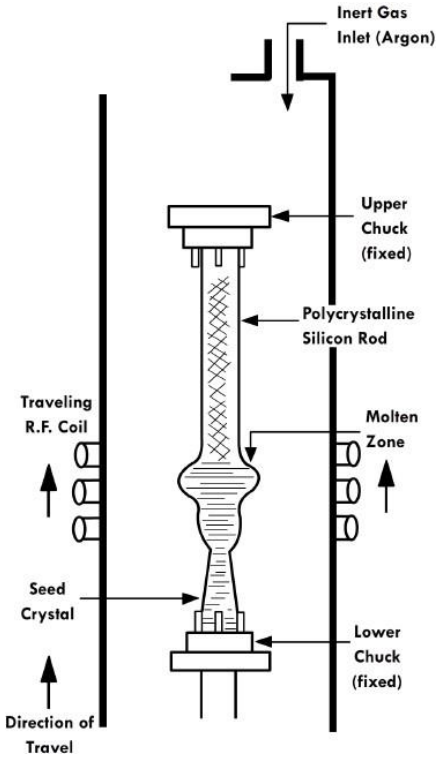
1. Furnace
2. Crystal pulling mechanism
3. Ambient control – atmosphere
4. Control system

Disadvantages of Czochralski technique: 1. Forms SiO_2 precipitates (could be useful if used correctly: mechanical strength and internal gettering) and 2. At higher temperatures the inner lining of the crucible starts melting and needs to be replaced periodically.

Float zone technique: This is mainly used for small wafers. This technique is good for producing specialty oxygen impurity free wafers.

Three main components of the process:

1. A polycrystalline EGS rod is fused with single crystal Si seeds of desired orientation.
2. This is taken into an inert gas (to reduce gaseous impurities) furnace and melted along the rod length by a travelling RF coil.
3. When the molten region solidifies it takes up the crystallinity of the seed crystals.

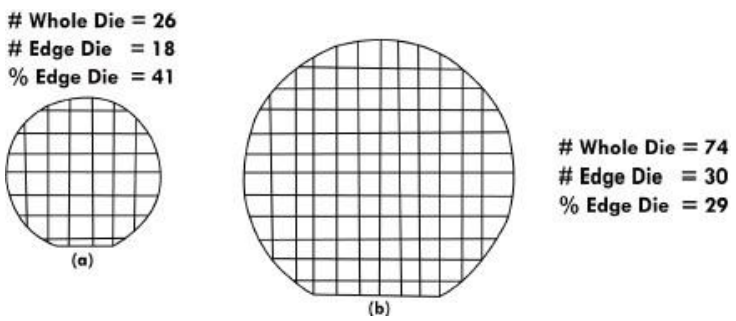


Disadvantages of float zone method: The process cannot be extended to large wafers (that are often required in IC industry) since it produces large number of defects. It is mainly used for specialty low oxygen impurity wafers.

Step 4: further processing to form wafers

1. The seed end (upper) and tang end (lower) are cut
2. The surface of the ingot is ground to get uniform diameter across length of ingot
3. Primary flat (identifying crystal orientation) and secondary flat (identifying dopant type and orientation) are cut.
4. The wafers are cut using diamond saw
5. Chemical etch to remove sawing damage.
6. The wafers are polished single side or double side using chemical mechanical polishing.

<u>Die yields in silicon wafers:</u>



Die yield is the extent to which a wafer can produce dies (percentage to total number of dies). Only whole dies are useful, so-called edge dies are not useful. The larger a die, how relatively less edge dies there are, which leads to greater die yields. Dies on which defects occur are neither useful. Defects exists due to factors as environment, chemicals, handling, and equipment. The main goal for highest die yield is to create wafers with (i) as small dies as possible, (ii) as much dies as possible and (iii) as least defects as possible.

<u>Yield calculation:</u>

$Ntotal = \frac{\pi(R-\sqrt{A})^2}{A}$, N = number of dies per wafer, A = chip area, D = defect density, R = wafer radius

$Y = e^{-\sqrt{AD}}$ Moore Model, the calculation of the total die yields

$Y = \frac{Ngood}{Ntotal}$, N_{good} is the number of working dies.

Lecture 5 & 6 – Thermal oxidation and masking

Silicon is unique for thermal oxidation for the following properties:

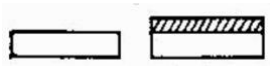
- Si is unique in the fact that its surface can be passivated with a native oxide
  - Layers are easily grown thermally
  - It has few defects
  - It is stable over time

- Its mechanical and electrical properties are almost ideal
  - Good adhesion
  - Prevents the penetration (in-diffusion) of dopants

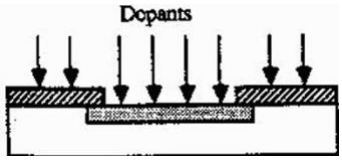
- Resistant to most chemicals used in fabrication
- Easily patterned and etched with specific chemicals or dry etched with plasmas

A silicon dioxide layer has the following critical uses in MEMS fabrication:

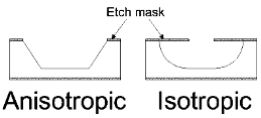
- Surface passivation
  - Preventing the silicon from dirt, scratches, and chemical reactions.



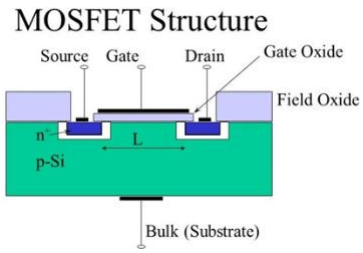
- Doping barrier
  - Silicon dioxide layer can block the dopant form reaching the silicon surface. The silicon dioxide thermal expansion coefficient is similar to silicon wafer. Therefore, thewafer with oxides will not warp (deform) during high temperature process



- Masking layer
  - See further on in this summary
- Etch stop layer
  - The etching (cutting out) of silicon stops at this layer



- Sacrificial layer
  - The layer is first created and then removed to create certain structures (such as a cantilever). See further on in this summary.
- Isolation of different regions
  - A field oxide isolates separate MOSFETs on a single wafer. Gates are the active regions on a MOSFET.



Silicon oxides at room temperature with a speed of 0.1 – 0.2 nm per minute. After a few hours this reaction stops with a layer of 1 – 2 nm thick.

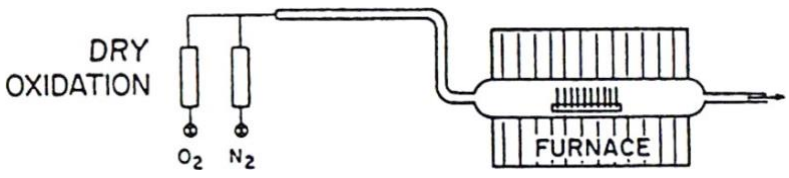
<u>Basics of oxidation:</u>

Oxidation could be done in two ways (ratio Si 45%:55% O_2 in SiO_2-layer):

Dry oxidation

Only oxygen (O_2) is used at 900 to 1200 °C: $Si(s) + O_2(g) \longrightarrow SiO_2(s)$. The layer is 0,05 – 0,5 μm thick (very thin). Could be done on top of wet oxidation to increase the quality. Used for gate oxides.

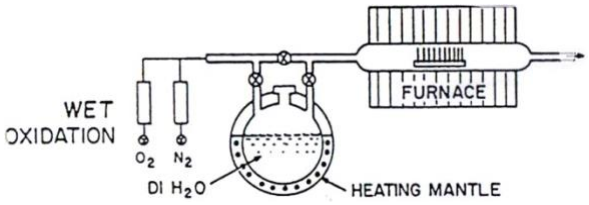
Advantages: Very high quality, excellent insulator
Disadvantages: Very thin, very expensive, low oxidation rate (takes long)



Wet oxidation

Water vapor (H_2O) is used: $Si(s) + 2H_2O(g) \rightarrow SiO_2(s) + 2H_2(g)$. The layer is up to 2,5 μm thick. H_2 is released as a side-product. Used for field oxides and masking.

Advantages: Quite thick, high oxidation rate (up to 600 nm/h), cheaper
Disadvantages: lower quality (due to H_2-creation), less good insulator

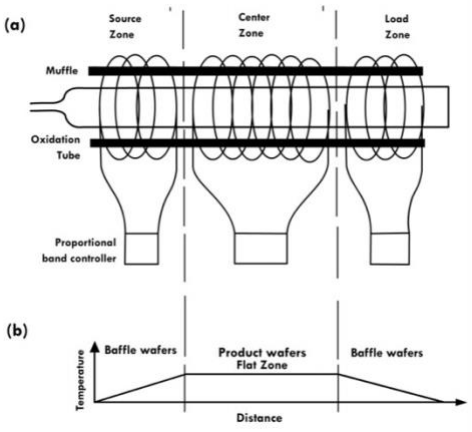


<u>Furnace:</u>

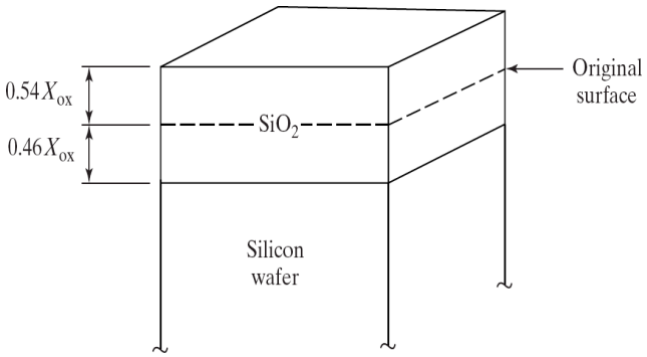
The furnace is divided in three parts (a):

1. Source zone (O_2/H_2O is introduced)
2. Center zone (oxidation occurs)
3. Load zone (wafers are loaded into the camber)

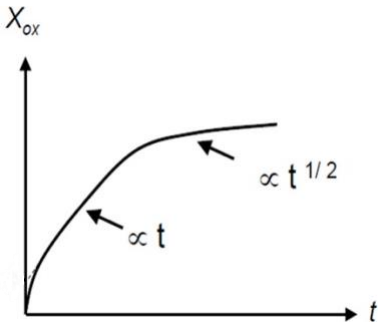
Each part has its own temperatures (b) variating from ± 300-400 °C to ± 900-1200 °C



Growth of the layer occurs 54% <u>above</u> and 46% <u>below</u> the original surface as silicon is consumed.



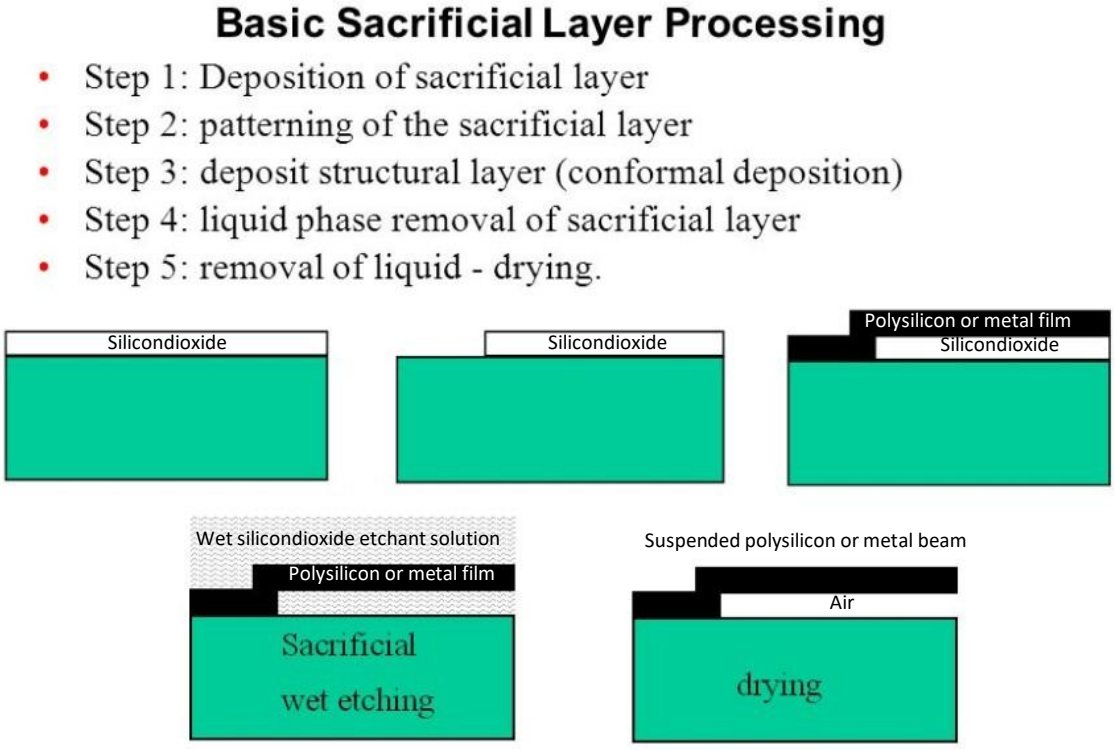
A layer is grown linearly in the beginning stage (i.e., the grow rate is constant). In a later stage the growth rate decreases over time, since the silicon surface is harder to reach for oxygen atoms due to the thicker silicon dioxide layer. The oxidation rate depends on the crystal orientation. <111> crystal planes have a higher oxidation rate than <100> because there is a higher number of surface atoms.



Lithography:

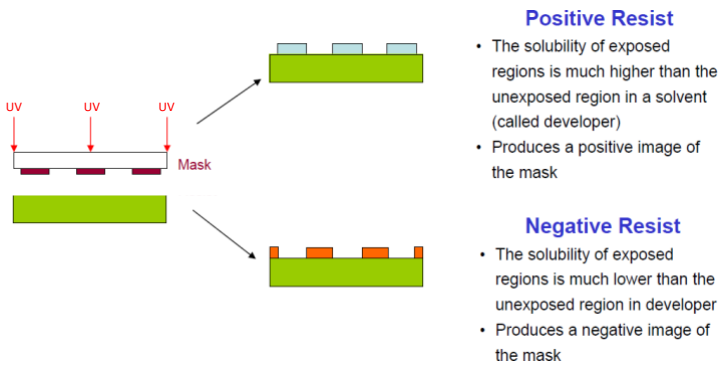
Lithography is a mechanism to print 2-D patterns to a thin film layer on a wafer surface. This is done by masks, which are made from glass (soda lime or quartz). The patterns are first transferred from the mask to photoresist (PR), a light-sensitive polymer. After opening windows in the PR, the pattern is transferred to the thin film using etching techniques.

Example of lithography (cantilever – sacrificial layer)



Photoresist:

Photoresist is an organic polymer which changes its chemical structure when exposed to ultraviolet (UV) light. It contains a light-sensitive substance whose properties allow image transfer onto a printed circuit board. There are two types of photoresists: (i) Positive (PPR): On exposure to UV light these resists become more soluble in developer (thickness of PPR is 500 nm – 10 µm) and (ii) Negative: On exposure to UV light these resists become less soluble in developer (thickness of PPR is 1 µm – 250 µm).



There are four components within a photoresist:

1. Polymer: this is a light sensitive polymer whose structure changes on exposure to light. The desired property is usually change in solubility in a specific solvent.
2. Solvent: The solvent is used to thin the photoresist so that it can be spin-coated on what wafer. The solvent is usually removed by heating to around 100 ^{0}C, called as soft bake process.
3. Sensitizers: These are used to control the chemical reaction during exposure.
4. Additives: Various chemicals that are added to achieve specific process results, like dyes.

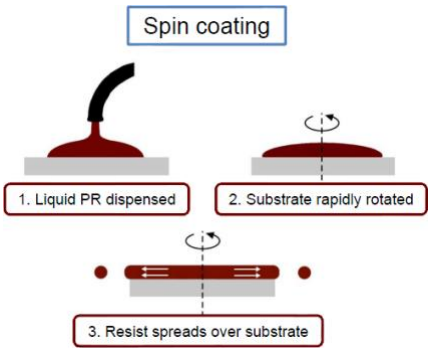
Positive PR vs. Negative PR

Property	Positive Photoresist	Negative Photoresist
Resolution	High	Low (~> 1um)
Developer	Temperature sensitive (-)	Temperature non-sensitive (+)
Mask Type	Dark-Field Mask: lower-defect	Clear-Field Mask: higher-defect
Rinse	In Water (+)	In solvent (n-Butylacetate) (-)
Cost	More Expensive	Cheaper
Exposure Speed		3-4 times faster (+)
Adhesion		Better
Backing	In air (+)	In Nitrogen (-)
Profile	Undercut (+)	Overcut (-)
Lift-off	In Acetone	In solvent (Methyl Ethyl Ketone) (-)

Lecture 7 & 8 – Masking & Lithography

<u>PR coating by spinning:</u>

A PR coating could be formed by spinning. First a liquid PR is dispensed on a round surface, which is rotated to form a film. This is hardened to form a coating.



Advantages: simple process, thick film
Disadvantages: shrinkage, less dense, more susceptible to chemical attack.
Common flaws in spin coating: particle contaminants, uncoated areas, air bubbles.

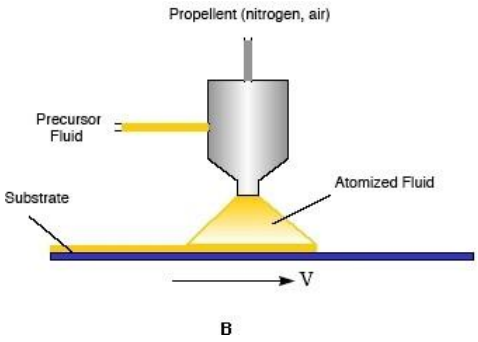
Properties from most important (1) to least important (6):
Photoresist properties: Viscosity (1), drying characteristics (3), dispense volume (5)
Spin properties: Spin speed (2), acceleration time (4), spin time (6)

$$z = \frac{kP^2}{\sqrt{\omega}}$$

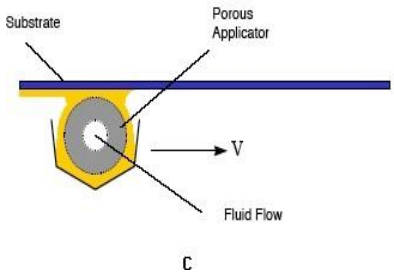
where z = film thickness in microns
P = % solids in resist
ω = angular velocity
k = constant in microns/sec$^{0.5}$

Other ways of PR coating:

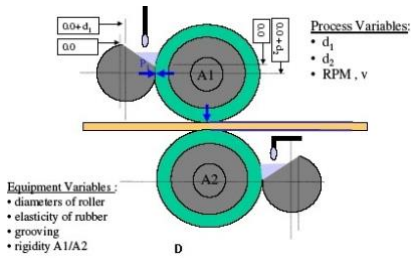
1. spray coating



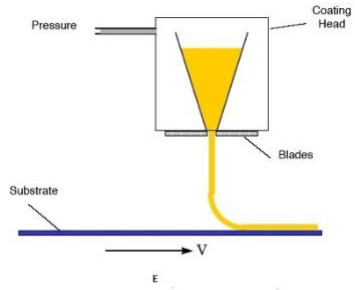
2. Contact roller coating (one side)



3. Contact roller coating (both sides)



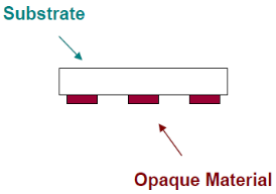
4. Dry resist film lamination



Masking in Lithography:

A photomask is an opaque plate with holes and/or transparencies which allow light to shine through in a defined pattern. A photomask is typically made of two materials: (i) **Glass**: Highest quality – chromium on fused quartz written with an electron beam exposing an electron-beam resist (PMMA) and (ii) **Plastic**: patterns printed from an AutoCAD file on transparencies with a very-high-resolution printer (lower resolution than glass, but cheap and fast).

The **substrate** in masking in lithography requires the following features:



- High transmission at exposure wavelength (UV, 365 nm)
- Small thermal expansion coefficient
- High degree of flatness
- Low non-linear effect

The **opaque material** in masking in lithography requires the following features:

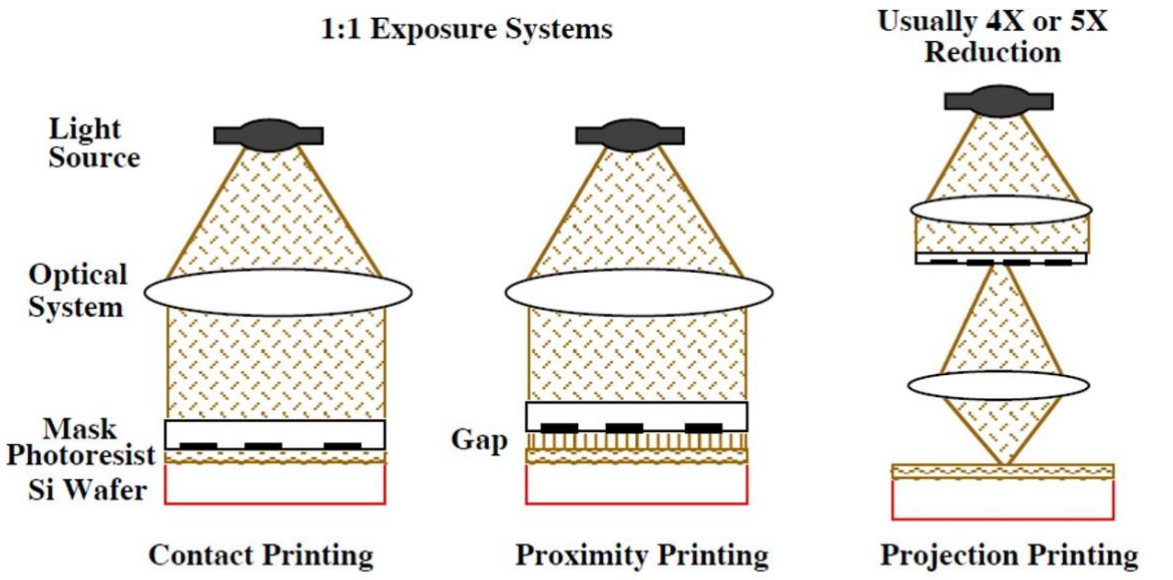
- No transmission at exposure wavelength
- Good adhesion to the substrate
- High degree of durability

Three types of mask polarity (orientation):

Dark-Field (negative) Grating Clear-Field (Positive)

Dark-Field Mask:
- Less adjacent/background exposure
- Less defect impact

Three basic types of lithographic wafer exposure systems:



High resolution, but mask wear generation. Fast, simple and inexpensive. Choice for R&D.

Less mask wear /contamination, less resolution (depend on gap).

No mask wear/contamination, resist features 4× smaller than mask. Very expensive, mainly used for IC industry.

Feature size:

Companies use the term “feature size” as a parameter to measure and denote the advancement in fabrication process. The smallest feasible pattern in lithographic fabrication is called the feature size. The smallest pattern is limited by the wavelength of the light used (typically few hundred nm). Electronic beams (e-beam) could theoretically improve the resolution, since it has a much smaller wavelength (few nm). In e-beam no mask is involved since the pattern is directly written on the wafer. Hence, it is a time-consuming and expensive process. The smallest feature size could be calculated by:

$$\sigma = k \frac{\lambda}{NA}$$

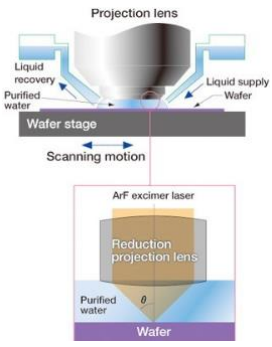
where σ is the feature size, k is Rayleigh constant (value of 0.5), is the wavelength and NA is the numerical aperture of the lens system.

The feature size could be reduced through the following techniques:

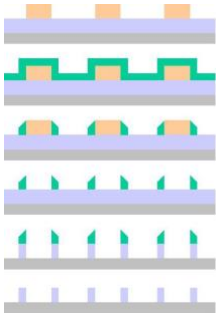
1. **Reduce the wavelength**
   For example, by X-ray lithography. However, for X-ray gold masks are required since X-ray has a higher penetration power. Thereby, other lenses need to be used. Therefore, it would be very expensive.

2. **Increase the refractive index of medium**
   NA = μ sinα where μ is the refractive index of the medium between the lens and the wafer. α is the semi-angle of the exit lens. To increase NA, μ can be increased, this is called *Immersion Lithography*.

3. **Immersion Lithography**
   Immersion Lithography uses purified water as the medium to increase NA and increase the resolution.



4. **Double patterning**
   Steps in double patterning. Side-wall spaces and an etching step is used to create patterns that are half of what can be achieved by the lithography setup.



Photoresist development:

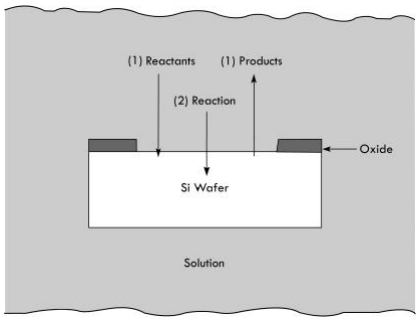
After alignment and UV exposure, the wafers must be developed. The wafers are dipped (wet process) into developer solution that reacts with the exposed photoresist, until the resist is completely removed. After an inspection, the substrate is “hard baked”, in which also additional solvents evaporate. Then the top layer of the wafer is removed through etching. Finally, the photoresist is removed, either by a wet process (acid mixture is used to remove the photoresist) or by a dry process (oxygen plasma is used to remove the resist).

Etching:

Etching is defined as: *selective removal* of solid material through chemical (or physical) reaction and can be done in two ways:

1. **Wet etching:**

   The wafers are immersed in a tank of the etchant. The etchant etches the silicon surface at selective regions through mask of silicon dioxide (or silicon nitride). *Step 1*: reactants are transported to the surface of the wafer. *Step 2:* Etching takes place. *Step 3:* by-products are removed. Wet etching is easier and simpler than dry etching. Moreover, it has a higher selectivity and a higher etch rate.



2. **Dry etching**

   In dry etching wafer get placed in a reactor where the etchant is a plasma flowing gas. Dry etching is considered as hard to control (not reproducible). On the other hand, dry etching has a higher degree of anisotropy, is easier to start and stop and is easier to automate than wet etching. Moreover, in dry etching safe non-toxic gases are used, where in wet etching corrosive liquids are used. Dry etching is however more expensive and less easy.

Etch rate:

The step in wet etching that takes the longest is called the rate-limiting step.

The etch rate has a higher dependence on temperature in a rate-limited etching process than in a diffusion-limited etching process. The depence between etch rate and temperature can be defined by the Arrhenius equation:

$R = R_0 e^{-E_A/kT}$ *, where R_0 is the rate constant that depends on the density and diffusivity of reactants, EA is the activation energy, and k is the Boltzmann constant. To obtain parameters of the Arrhenius equation, a graph is plotted for ln R vs 1/T. The slope of this graph is (-EA/k) and the pre-exponential factor R0 is obtained from the intercept of this graph*

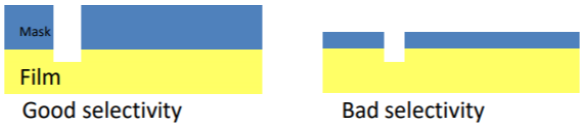
The etch rate has a high dependence on agitation (disturbance of a liquid) in a diffusion-limited etching process.

Generally, considering the Miller-indices <110> and <100> directions have a (much) higher etch rate than the <111> directions.

Selectivity:

The ratio of etching rate (V) between different materials is usually the higher the better. Selectivity is the ratio of the etch rate of the layer being etched to the etch rate of the mask layer (or the layer under the layer being etched). Selectivity is calculated by:

$$S_{fm} \equiv \frac{V_{f\perp}}{V_{m\perp}} (vertical\ components\ only)$$

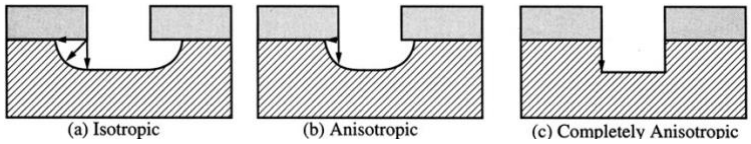


The higher the selectivity, the better the film and mask layer could be used for etching.

Isotropic and anisotropic etching:

In *isotropic* the etch rate is the same along all directions, while in *anisotropic* the etch rate depends on the direction. The *isotropic rate* is defined by:

$$Ri = \frac{Horizontal\ Etch\ Rate\ (Rh)}{Vertical\ Etch\ Rate\ (Rv)}$$



In isotropic etching Ri = 1, in anisotropic etching Ri < 1 and in complete anisotropic etching Ri = 0. In isotropic etching the pattern dimension is poorer defined than in anisotropic etching.

Isotropic:

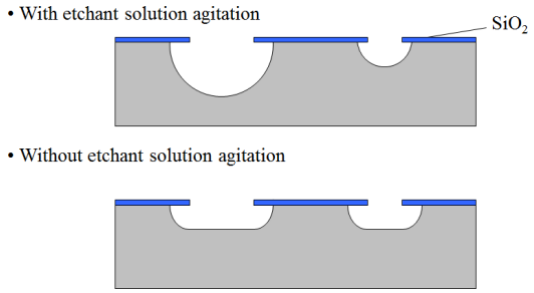
Best to use with large features when sidewall slope does not matter, which additionally makes it also easier to lift off the mask. There is large loss in critical dimension (CD, i.e., feature size). Isotropic etching is overall quick, easy, and cheap.

Anisotropic:

Best for making small features with vertical sidewalls, preferred pattern transfer method for nanofabrication and some micro-fabrication. Is typically more expensive.

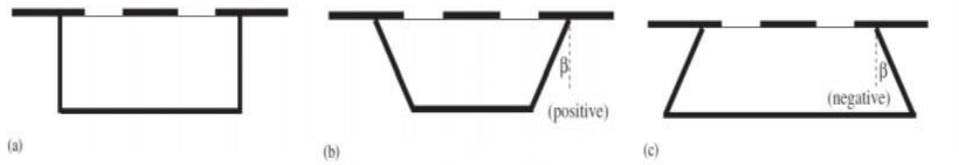
Underetching occurs if the surface profile is etched incompletely. A rough oxide layer is left behind due to the local variations in the rate of removal of the oxide layer. **Overetching** occurs when too much resist is etched. This could cause damage to the wafer and could cause the resist to lift off.

Agitation is defined as the movement or disturbance of the etchant liquid during wet etching. The shape of the etching changes if agitation occurs as shown in the figure on the right.



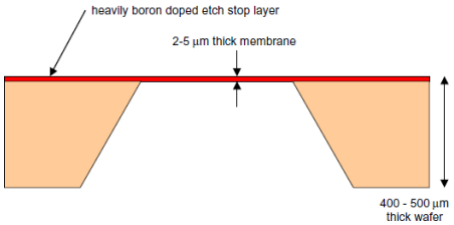
The shapes of the side walls depend on the orientation of the etched materials and etching conditions. This is called the **etching profile**:

- Rectangular-shaped sidewalls can lead to reduced conformal thickness and causes discontinuous films
- Gradual positive sloping allows continuous interconnection metal to be deposited
- Negative sloping sidewalls, depositing continuous thin films is not possible.



Etching sidewall shapes: (a) rectangular-shaped, (b) positive sloping, and (c) negative sloping [4].

In wet etching it is very hard to control where the etching should stop. Therefore, often a **wet etch stop is used**. This is a thick membrane which is heavily doped in boron. This causes the etching to stop at a given point.



<u>Etchants used in wet silicon etching:</u>

<u>Isotropic</u>

(1) $HF:HNO_3:CH_3COOH:H_20$ (2) HF
(3) $HF:NH_4F$

<u>Anisotropic</u>

(1) KOH (2) EDP (Ethylenediamine Pyrocatechol)
(3) CsOH (4) NaOH (5) N_2H_4-H_20 (Hydrazine)

<u>Masking Materials</u>

(1) Photoresist (Acids Only) (2) Si_3N_4
(3) SiO_2